AMENDMENTS TO THE CLAIMS:

1. (Previously amended) A wafer comprising:

a base layer;

an active layer formed on the base layer;

a gate dielectric layer formed on the active layer;

a conductive layer formed on the gate dielectric layer; and

a plurality of isolation regions formed in said wafer,

said wafer being divided into a plurality of first portions, second portions, and third portions;

said first portions comprise gate dielectric capacitors, said gate dielectric capacitors comprise a first electrode layer, an insulating layer, and a second electrode layer; wherein the first electrode layer is formed from said active layer, the insulating layer is formed from said gate dielectric layer, and the second electrode layer is formed from said conductive layer;

said second portions comprise first dummy structures, said first dummy structures comprise a first electrode layer and an insulating layer; wherein the first electrode layer of the first dummy structures is formed from said active layer and the insulating layer of the first dummy structures is formed from said gate dielectric layer, wherein said second portion does not contain said conductive layer; and

said third portions comprise second dummy structures, said second dummy structures comprise an insulating layer and a second electrode layer; wherein the insulating layer of the second dummy structures is formed from an isolation region and the second

electrode layer of the second dummy structures is formed from said conductive layer, wherein said third portion does not contain said active layer.

2. (Original) The wafer of claim 1, wherein the isolation regions are shallow trench isolation regions.

3. (Original) The wafer of claim 1, wherein said conductive layer comprises polysilicon.

4. (Original) The wafer of claim 1, wherein said active layer comprises doped silicon.

5. (Original) The wafer of claim 1, further comprising an interconnect layer formed over said conductive layer.

6. (Original) The wafer of claim 5, wherein said interconnect layer comprises a metal.

7. (Cancelled)

8. (Previously amended) The wafer of claim 1, further comprising a silicon electrode contacting an isolation region.

9. (Cancelled)

10. (Original) The wafer of claim 1, wherein said gate dielectric capacitor is a transistor.

Claims 11-20 (Withdrawn)

21. (Currently amended) ~~The~~ A wafer ~~of claim 4,~~ comprising:

a base layer;

an active layer formed on the base layer;

a gate dielectric layer formed on the active layer;

a conductive layer formed on the gate dielectric layer; and

a plurality of isolation regions formed in said wafer,

said wafer being divided into a plurality of first portions, second portions, and third portions;

said first portions comprise gate dielectric capacitors, said gate dielectric capacitors comprise a first electrode layer, an insulating layer, and a second electrode layer; wherein the first electrode layer is formed from said active layer, the insulating layer is formed from said gate dielectric layer, and the second electrode layer is formed from said conductive layer, wherein said active layer comprises source/drain regions;

said second portions comprise first dummy structures, said first dummy structures comprise a first electrode layer and an insulating layer; wherein the first electrode layer of the first dummy structures is formed from said active layer and the insulating layer of the first dummy structures is formed from said gate dielectric layer, wherein said second portion does not contain said conductive layer; and

said third portions comprise second dummy structures, said second dummy structures comprise an insulating layer and a second electrode layer; wherein the insulating layer of the second dummy structures is formed from an isolation region and the second electrode layer of the second dummy structures is formed from said conductive layer, wherein said third portion does not contain said active layer.

22. (Previously added) The wafer of claim 8, wherein said silicon electrode is an electrically isolated polysilicon electrode that contacts an isolation region of the second dummy pattern.

23. (New) A wafer comprising:

a base layer;

an active layer formed on the base layer;

a gate dielectric layer formed on the active layer;

a conductive layer formed on the gate dielectric layer; and

a plurality of isolation regions formed in said wafer,

said wafer being divided into a plurality of first portions, second portions, and third portions;

said first portions comprise gate dielectric capacitors, said gate dielectric capacitors comprise a first electrode layer, an insulating layer, and a second electrode layer; wherein the first electrode layer is formed from said active layer, the insulating layer is formed from said gate dielectric layer, and the second electrode layer is formed from said conductive layer, wherein said gate dielectric layer is located between said first electrode layer and said second electrode layer;

said second portions comprise first dummy structures, said first dummy structures comprise a first electrode layer and an insulating layer; wherein the first electrode layer of the first dummy structures is formed from said active layer and the insulating layer of the first dummy structures is formed from said gate dielectric layer, wherein said second portion does not contain said conductive layer; and

said third portions comprise second dummy structures, said second dummy structures comprise an insulating layer and a second electrode layer; wherein the insulating layer of the second dummy structures is formed from an isolation region and the second electrode layer of the second dummy structures is formed from said conductive layer, wherein said third portion does not contain said active layer.